White Paper

Redpine Signals Differentiate with Ultra-Low Power Design

Venkat Mattela, CEO Redpine Signals

April 2007

Redpine Differentiates with Ultra-Low-Power Design

Redpine Signals' expertise is ultra-low-power design – from algorithm to silicon implementation. Venkat Mattela, chief executive officer, explains how Synopsys tools provide a robust and accurate low-power design flow that meets their current and future design needs.

Our target market is the competitive world of ultra-low-power wireless convergence products.

Because we operate in a highly competitive environment, we have to be very clear about the business value that we offer. Underpinning that business value is innovative design and efficient, low-power implementation.

The link between technology and business success is clear to see. The low-power optimizations we have achieved within our low-power design flow helped to improve the end-product differentiation on a wireless LAN core. This was a key factor in influencing two customers to select our technology over competitive solutions. Our customers, leading equipment and device manufacturers, need superior battery life as well as excellent wireless range and data rates.

Low Power from Architecture to Implementation

The company's wireless platforms are built upon differentiating technology that includes ultra-low-power OFDM (Orthogonal Frequency Division Multiplexing) and MIMO (Multiple-Input-Multiple-Output)-based wireless architectures, as well as multi-threaded processing engines. The implementation of standards-compliant wireless technology enables us to deliver application-aware ultra-low-power wireless connectivity. In essence, our architectures are designed for low power from the outset.

When operating at suboptimal ranges or in hostile environments, wireless communication systems often downshift to lower data rates to improve reliability. This results in excessive battery drain for the transfer of a given amount of data. To counter this we aim to improve the efficiency of our IP's wireless performance without a major increase in chip size. This requirement is a strong driver for adopting a low-power design flow.

As a fabless vendor, it's vitally important that we achieve optimal semiconductor implementation into the target process geometry. The effort we put into semiconductor implementation gives us an additional competitive edge, and is a further opportunity to optimize for power. This is where we look to Synopsys for a low-power implementation solution that enables our designers to achieve the design goals we set.

Benchmark Evaluation

The Redpine design team has completed a number of designs with Synopsys' implementation and verification tools, and has a good understanding of how to get the best results from them. As part of the adoption process for our low-power methodology, we undertook an extensive benchmarking exercise that included the implementation of a test chip.

We set two goals for the evaluation: first, to see how much power could be saved by applying optimizations during implementation, and second, to verify the power sign-off accuracy by comparing the output from the analysis tools against the test chip. Support from the local Synopsys technical team while we ran the evaluation ensured that we got the best out of the tools and that the exercise was completed quickly.

Our design team used Power Compiler™ to synthesize clock-gating and perform gate-level power optimization. At low levels of activity – just one percent of nodes toggling – the optimized design reduces dynamic power by almost 17 percent compared to the original design and reduces area by almost five percent. With 50 percent of nodes toggling, the dynamic power is reduced by over 66 percent while the area saving is over five percent (see Table 1).

Switching activity	Dynamic Power Savings	Area Savings
1% nodes toggling	16.86%	4.86%
50% nodes toggling	66.45%	5.46%

Table 1. Power Optimization Results

The results of the PrimeTime® PX analysis are equally impressive. Depending on which period of simulation activity is measured, the correlated difference with the measured silicon varies between 0.5 percent and 1.7 percent (Table 2). This is well within the target limits set by our engineers.

Simulation Timing Window	Correlated difference with test chip
1/4 to 3/4	1.7%
1/5 to 4/5	0.5%

Table 2. PrimeTime PX Correlation with Test Chip Silicon

Multi-Voltage Future

In moving to more advanced technologies – 90nm and 65nm processes – the power challenge changes once again. At these geometries we must move forward more aggressively with advanced power-saving techniques that minimize leakage power as well as dynamic power. The fact that the Synopsys low-power implementation and verification solution supports advanced low-power techniques today was a further factor in our decision to use their solution.

Multi-voltage design techniques can help reduce both leakage and dynamic power consumption by minimizing the supply voltage level or completely shutting it down wherever possible. One of the designer's tasks in implementing a multi-voltage design is to specify power domains. These logically group blocks that share the same power behavior. Special library cells are then used to step the voltage between different power domains, or completely isolate those domains that can be shut down for periods of time.

Manual implementation of multi-voltage chips is possible, but like all chip design tasks, automation is much preferred as it speeds the design process and reduces the possibility of introducing errors. Automatically handling multi-voltage implementation in the design flow requires that the entire flow is multi-voltage aware. Synopsys has added multi-voltage features to RTL synthesis, test synthesis, physical implementation, and formal verification, static timing analysis and sign-off.

Core Expertise

Our customers will continue to demand products that offer the lowest possible power and area figures while meeting the required performance. Low-power design is a core competence within Redpine Signals and we will continue to develop those skills as we develop new algorithms, design innovative architectures and implement them in silicon using low-power design flows.

Venkat Mattela, Chief Executive Officer

Mr. Mattela has over 23 years of engineering and management experience in the semiconductor industry. Prior to joining Redpine, Mr. Mattela was Director responsible for the product, strategy and business development for media wireless connectivity solutions at the Network Media Platforms Group of Analog Devices. Prior to that, Mr. Mattela was a Director at Infineon Technologies, responsible for micro-architecture definition and design of TriCore MCU-DSP processor. He started his career at Tata Institute of Fundamental Research, India and held various engineering positions at LSI Logic, LMSI and CMC Ltd. He has a Masters Degree in Computer Sciences from Jawaharlal Nehru Technological University, India and holds 11 US patents.

About Redpine Signals

Redpine Signals is a fabless semiconductor company with a mission to create ultra-low-power wireless convergence products targeting next generation mobile and consumer applications.

Redpine Signals' experienced team has developed multiple patent-pending implementations of standards compliant wireless technology to deliver application aware ultra-low-power wireless connectivity which dramatically improves battery life on mobile devices as well as uses advanced MIMO techniques to improve robustness, range, and data-rate.

The company is headquartered in San Jose, California and has a state-of-the-art development center in Hyderabad, India.

Web Links

Redpine Signals
http://www.redpinesignals.com/

SYNOPSYS®

700 East Middlefield Road, Mountain View, CA 94043 T 650 584 5000 www.synopsys.com