

# Perform low-power manufacturing test

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The very process of testing digital circuits routinely increases their dynamic power consumption to levels exceeding their power specification. If the power consumption is great enough, it can result in failures at wafer probe or pre-burn-in package test that require a significant amount of time and effort to debug. This issue, especially prevalent when testing very large SoCs under corner conditions, causes unnecessary yield loss on the production line and reduces manufacturers' gross margins. The best way to avoid test power problems is to incorporate power-aware testing techniques in the design-for-test (DFT) process. This article examines the relationship between dynamic power consumption and test to determine why managing power is more critical today than ever before. It also explores two DFT methodologies that take advantage of recent advances in ATPG technology to automate the generation of low-power manufacturing tests.

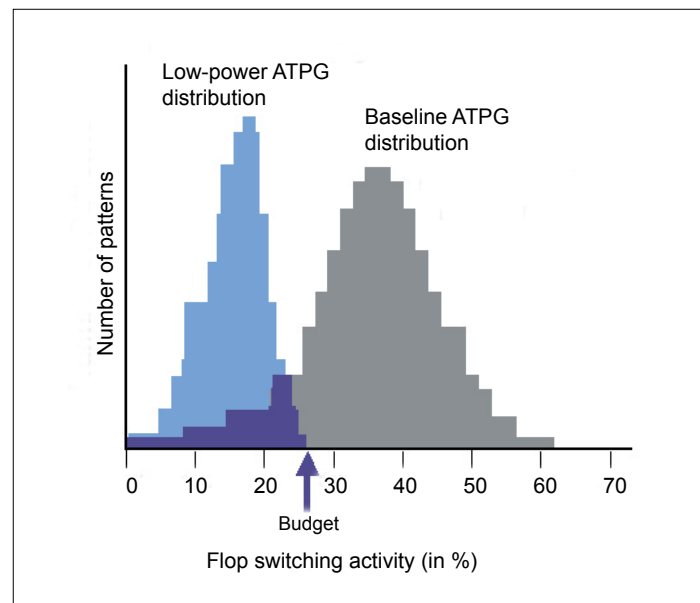
## Test power issues

Scan ATPG algorithms are optimized to reduce the number of patterns, which means that each pattern improves fault coverage as much as possible. Bits in the scan pattern that set up and propagate the targeted faults are called "care bits." The remaining bits are randomly filled to detect additional "bonus" faults not explicitly targeted by the care bits. Both care bits and random-fill bits in each scan pattern cause logic state transitions that charge and discharge parasitic capacitors in a device. This increases dynamic power relative to the level con-

sumed when the circuit operates under normal conditions.

There are two types of dynamic power consumption that affect device testing: peak power and average power. Peak power, also called "instantaneous power," is the amount of power consumed during a small period of time such

power rails introduces undesirable circuit delays. Sometimes, scan data fails to propagate to the next stage in the scan chain, resulting in test program failure. Power rail droop in shift mode is usually addressed by reducing the scan shift frequency sufficiently to allow enough time



Since both the peak and mean switching rates exceed 26 percent, there is substantial risk that scan testing will increase IR-drop delays relative to normal device operation.

as the portion of a clock cycle immediately following the rising (or falling) edge of the system clock. Peak power reflects the node switching activity level in a device: the more nodes that simultaneously switch from one logic state to another, the higher the peak power.

Scan testing can increase peak power in a device by up to 20x the level consumed with mission-mode patterns. Switching currents can be so pronounced that power rail collapse occurs: bits shifted into a circuit along a scan chain are dropped, resulting in pattern mismatches on the tester. Switching currents are less severe than this, but they can still cause power rail droop, whereby the increased IR-drop along

for scan signals to meet the shift cycle timing under corner conditions. Reducing the scan shift frequency, however, increases tester time and hence, test cost in volume production.

Even if a pattern is successfully scanned in, peak power during the launch/capture sequence (called "capture mode") can contribute enough IR-drop delay that logic values fail to transition within the capture window and the device fails the pattern. Although this issue is associated with both stuck-at and transition delay tests, it is more common in delay-dependent at-speed test patterns. The IR-drop problem in capture mode and the power rail collapse problem in shift mode can be addressed by overde-

sign of the power rail system to accommodate the increased switching activity of scan testing. Yet increasing the width of power and ground rails adds area to the circuit that would be unnecessary if there were better ways to control peak test power.

Average power is power consumption averaged over a large number of clock cycles, such as the hundreds or thousands of cycles needed to scan a single stimulus pattern into a design while scanning out the response to the previous pattern. Scan testing can increase average power in a device by two to five times the level consumed with mission-mode patterns. Excessive average test power can lead to thermal problems such as "hot spots" on the die that can damage the device. Because average power is directly proportional to frequency, it can be controlled during scan shifting by selecting a shift frequency low enough to avoid the problem. As noted, reducing the scan shift frequency can contribute to higher test cost.

Because average test power is relatively straightforward to manage on the tester, most power-related test issues today stem from excessive peak power. Unobtrusive ways to reduce both peak power and average power during test is currently the focus of efforts in the semiconductor and design automation industries.

## Detecting nm defects

Managing power consumption during test is important because the latest fabrication processes enable the manufacture of designs containing hundreds of thousands—even millions—of scan flops. A large portion of these flops can simultaneously switch during scan testing and this peak switching activity increases peak power and exacerbates IR-drop delays.

Moreover, because defect densities for processes at 65nm and below have increased, product yields have decreased. To compensate for these lower yields and maintain acceptable quality levels, manufacturers are turning to ultrahigh-resolution at-speed testing to detect very small delay defects inside devices. The enhanced timing resolution capable of using small delay defect ATPG is effective in detecting nanometer defects previously undetectable using standard transition delay testing. However, the technique requires even tighter control of incidental delays caused by peak currents generated during test than standard at-speed test methods.

Very large SoCs now rely on advanced at-speed ATPG tech-

nologies to maintain high test quality in the presence of more nanometer defects, and this trend is driving the use of power-aware testing techniques in the DFT flow.

### **Power reduction**

Flop switching activity is highly correlated with node switching activity, and dynamic power consumption reflects node switching activity. It is thus reasonable to conclude that reducing flop switching activity sufficiently during scan test is an effective way to avoid power-related failures caused by test. Detailed case studies of IR-drop behavior in fabricated devices support this observation. The goal of power reduction techniques, then, is to reduce flop switching activity

sufficiently so that “good” devices pass all scan ATPG tests under corner conditions. Notice we do not need to minimize switching activity, but just reduce it to levels comparable with switching rates observed when mission-mode patterns are applied.

To illustrate, assume we apply a large number of mission-mode patterns to a design and find that the peak flop switching activity is 26 percent of the total number of flops. If we generate scan ATPG patterns and track the number of patterns corresponding to a given switching rate, we might observe a distribution similar to the grey distribution in the Figure. Since both the peak and mean switching rates exceed 26 percent, there is substantial risk that scan testing will increase

IR-drop delays relative to normal device operation.

If, however, we employ techniques to reduce power consumption during test, we effectively shift the distribution to the left. In the overlapping blue low-power distribution of the Figure, the peak switching activity of the scan ATPG patterns doesn't exceed the power budget, so the risk of power issues occurring during manufacturing test is diminished.

In the next issue, we'll look at two approaches to achieving low-power pattern distributions. They differ fundamentally in the manner in which the power budget is specified.

*(This is the first part of a two-series article. Part two will follow in the next issue.)*